4

Docket No.: 04303/100N147-US1

AMENDMENTS TO THE CLAIMS

Claims 1-5: (Canceled)

Claim 6 (Presently Amended): A searcher device for correlating a first code sequence with a second code sequence, the searcher comprising:

a memory for storing the first code sequence; and

a plurality of computation circuits coupled to the memory, wherein each of the plurality of computation circuits performs a correlation operation between the first code sequence and the second code sequence at a unique phase offset The searcher recited in Claim 1, and

wherein each of the plurality of computation circuits has a unique coupling offset from each other with respect to a location in which they are coupled to the memory.

Claims 7-16 (Canceled)

Claim 17 (Original): <u>In a searcher, a method of determining a phase offset of a signal, the method comprising the steps of:</u>

a) receiving the signal having a first code sequence in a memory;

b) receiving an additional signal having a second code sequence at a plurality of computation circuits;

Application No.: 09/751,777

Docket No.: 04303/100N147-US1

c) implementing a unique phase offset for the second code sequence in each of the plurality of computation circuits by wherein offsetting step c) comprises the following step:

5

loading the second code sequences in the plurality of computation circuits, wherein the plurality of computation circuits are each coupled in an offset manner with the memory; and

d) correlating the second code sequence having the unique phase offsets with the first code sequence in each of the respective plurality of computation circuits The method recited in Claim 12.

Claim 18 (Original): In a searcher, a method of determining a phase offset of a signal, the method comprising the steps of:

a) receiving the signal having a first code sequence in a memory;

b) receiving an additional signal having a second code sequence at a plurality of computation circuits;

c) implementing a unique phase offset for the second code sequence in each of the plurality of computation circuits by The method recited in Claim 12 wherein offsetting step c) comprises the following step: temporarily storing the second code sequence in a memory buffer with varying size to provide the unique phase offset to each of the plurality of computation circuits; and

d) correlating the second code sequence having the unique phase offsets with the first code sequence in each of the respective plurality of computation circuits.

Claims 19-25 (Canceled)

Docket No.: 04303/100N147-US1

Claim 26 Original): A communication device for processing data signals, the communication device comprising:

a transceiver for receiving a signal having a first code sequence;

a code generator for generating a second code sequence;

a searcher coupled to the transceiver and to the code generator, the searcher having a plurality of computation circuits for correlating in parallel the first code sequence and the second code sequence at a plurality of offsets; and The communication device recited in Claim 23 further comprising:

at least one memory block coupled to at least one of the plurality of computation circuits, the memory block having a variable length to implement a variable offset between the first code sequence and the second code sequence.

Claim 27 (Canceled)

Claim 28 (Newly Added): A searcher device for correlating a first code sequence with a second code sequence, the searcher comprising:

a memory for storing the first code sequence;

a plurality of computation circuits coupled to the memory; and

a plurality of offset code sequence generators that are coupled respectively to the plurality of computation circuits and generate the second code sequence at unique phase offsets,

{W:\04303\100N147000\00162890.DOC|@@@@@@@@@@@@@@@@}}

Application No.: 09/751,777

7

Docket No.: 04303/100N147-US1

wherein each of the plurality of computation circuits performs a correlation operation between the first code sequence and the second code sequence at a unique phase offset.